

web: <http://www.ant-audio.co.uk>
email: info@ant-audio.co.uk

Application of indirect negative feedback in FET voltage amplifiers.

Indirect negative feedback is a very old linearisation technique, used in valve circuits many years ago and not uncommon in modern ICs. It also can be very useful in voltage amplifier circuits using modern JFET and MOSFET devices (though the idea is easily applicable to valve circuits using high-gain valves – i.e. pentodes). Let's compare two circuits with the same gain and exactly the same input stage shown on Fig 1. In the first circuit the output voltage distortion mirrors the distortion of the drain current of J3 as the gain is defined by R11 and the second FET J4 acts just as a current source. In the second circuit the J2 drain current is modulated by the output voltage through the indirect feedback loop R1+R2. As a result the output voltage distortion are greatly reduced – as would be the case with a more usual direct NFB application. A simplified way to understand how the circuit works is this – the drain current of the lower FET J1 $I_{d1} = F(V_{gs1})$, where F is the transfer function of the FET used and V_{gs1} – the gate-source voltage of the J1. If the currents through the resistive network R1+R2 and the load are negligible than the drain current of the top FET J2 $I_{d2} = I_{d1}$. For two identical FETs (and providing that the drain current is largely independent of the source-drain voltage), the gate-source voltages of both FETs V_{gs1} and V_{gs2} would be almost the same for all values of the drain current I_{d1} . Now, the change in the input voltage ΔV_{gs1} would create the same change in the gate-source voltage of the top FET ΔV_{gs2} . That voltage is, in turn, defined by the output voltage V_{out} through the indirect feedback loop R1 and R2, $\Delta V_{gs2} = K \times \Delta V_{out}$, where $K = -(R1+R2)/R2$ – is the gain.

It is easy to see that in this ideal case the gain is almost not affected by the transfer function of the input FET J1 (as it should be the case for a very high open loop gain and exact match between two FETs) resulting in a linear voltage amplification despite a highly non-linear voltage to current transfer function of the FET J1. Real life FETs have a limited voltage gain, non-linear capacitances etc. Nevertheless it is possible to build a voltage amplifier stage using this approach with considerably lower distortion comparing to a standard circuit with the same gain. The simulated distortion for 200 mV p-p input and 10V p-p output are nearly 4% for the first circuit and only about 0.12% for the second circuit – 30 dB reduction illustrates very well potential benefits of this approach. I've used this idea in the VAS of the A.N.T. Audio Amber 3T headphone amplifier with very good results.

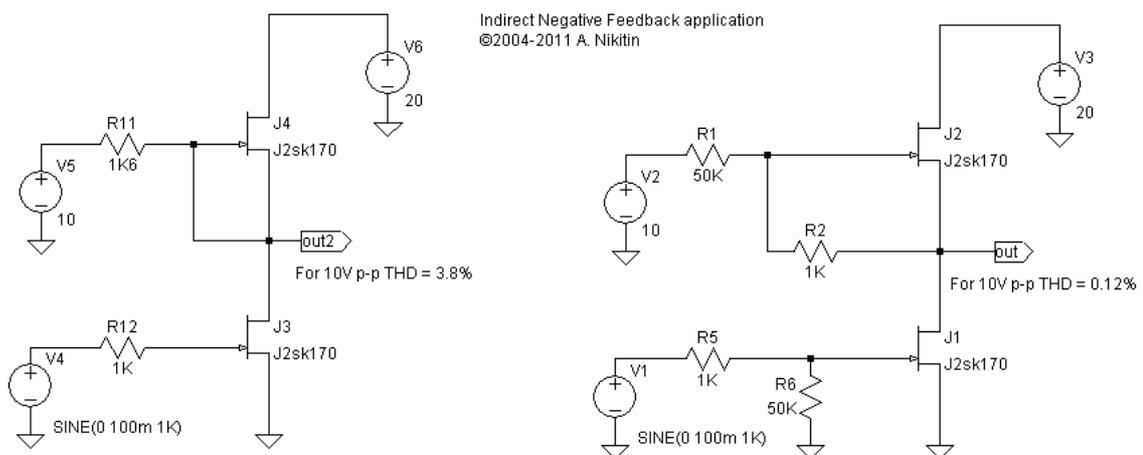


Fig1